LMH6584/LMH6585 32x16 400 MHz Analog Crosspoint Switches, Gain of 1, Gain of 2

Check for Samples: LMH6584, LMH6585

FEATURES

- **32 Inputs and 16 Outputs**
- **144-pin LQFP Package**
- **−3 dB Bandwidth (V_{OUT} = 2 V_{PP}, R_L = 150Ω) 400 MHz**
- **Fast Slew Rate 1200 V/µs**
- **Channel to Channel Crosstalk (10/100 MHz) −52/ −43 dBc**
- **Easy to Use Serial Programming 4 Wire Bus**
- **Two Programming Modes Serial & Addressed Modes**
- **Symmetrical Pinout Facilitates Expansion**
- **Output Current ±50 mA**

APPLICATIONS

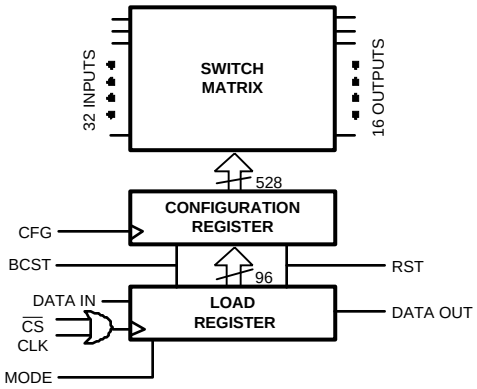
- **Studio Monitoring/Production Video Systems**
- **Conference Room Multimedia Video Systems**
- **KVM (Keyboard Video Mouse) Systems**
- **Security/Surveillance Systems**
- **Multi Antenna Diversity Radio**
- **Video Test Equipment**
- **Medical Imaging**
- **Wide-Band Routers & Switches**

DESCRIPTION

The LMH™ family of products is joined by the LMH6584 and the LMH6585 high speed, non-blocking, analog, crosspoint switches. The LMH6584/LMH6585 are designed for high speed, DC coupled, analog signals such as high resolution video (UXGA and higher). The LMH6584/LMH6585 have 32 inputs and 16 outputs. The non-blocking architecture allows an output to be connected to any input, including an input that is already selected. With fully buffered inputs the LMH6584/LMH6585 can be impedance matched to nearly any source impedance. The buffered outputs of the LMH6584/LMH6585 can drive up to two back terminated video loads (75Ω load). The outputs and inputs also feature high impedance inactive states allowing high performance input and output expansion for array sizes such as 32 x 32 or 64 x 16 by combining two devices. The LMH6584/LMH6585 are controlled with a 4 pin serial interface. Both single serial mode and addressed chain modes are available.

The LMH6584/LMH6585 come in 144-pin LQFP packages. They also have diagonally symmetrical pin assignments to facilitate double sided board layouts and easy pin connections for expansion.

Block Diagram



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
V_S		±6V
I_{IN} (Input Pins)		±20 mA
I_{OUT}		See(4)
Input Voltage Range		V^- to V^+
Maximum Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

Operating Ratings(1)

Temperature Range(2)		−40°C to +85°C
Supply Voltage Range		±3V to ±5.5V
Thermal Resistance (144-Pin LQFP)	θ_{JA}	22°C/W
	θ_{JC}	5°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$and θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

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±3.3V Electrical Characteristics[1]

Unless otherwise specified, typical conditions are: T_A = 25°C, V_S = ±3.3V, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[3]	Max[2]	Units
Frequency Domain Performance						
SSBW	−3 dB Bandwidth	LMH6584, V_{OUT} = 0.25 V_{PP}[4]		350		MHz
		LMH6585V, V_{OUT} = 0.5 V_{PP}[4]		350		
LSBW		LMH6584, V_{OUT} = 1V_{PP}, R_L = 1 kΩ[4]		375		
		LMH6585, V_{OUT} = 2V_{PP}, R_L = 1 kΩ[4]		375		
		LMH6584, V_{OUT} = 1V_{PP}, R_L = 150Ω[4]		375		
		LMH6585, V_{OUT} = 2V_{PP}, R_L = 150Ω[4]		375		
GF	0.1 dB Gain Flatness	V_{OUT} = 2 V_{PP}, R_L = 150Ω		50		MHz
DG	Differential Gain	R_L = 150Ω, 3.58 MHz/ 4.43 MHz		0.06		%
DP	Differential Phase	R_L = 150Ω, 3.58 MHz/ 4.43 MHz		0.04		deg
Time Domain Response						
t_r	Rise Time	LMH6584, 2V Step, 10% to 90%		2.0		ns
		LMH6585, 2 V Step, 10% to 90%		1.26		
t_f	Fall Time	LMH6584, 2 V Step, 10% to 90%		1.75		ns
		LMH6585, V Step, 10% to 90%		1.0		
OS	Overshoot	LMH6584, 2 V Step		0		%
		LMH6585, 2 V Step		5		
SR	Slew Rate	LMH6584, 2 V_{PP}, 20% to 80%		900		V/µs
		LMH6585, 2 V_{PP}, 20% to 80%[5]		1300		
t_s	Settling Time	2V Step, V_{OUT} within 0.5%		15		ns
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	LMH6584, 1 V_{PP}, 10 MHz		−70		dBc
HD3	3rd Harmonic Distortion	1 V_{PP}, 10 MHz		−75		dBc
e_n	Input Referred Voltage Noise	>1 MHz		12		nV/√Hz
i_n	Input Referred Current Noise	>1 MHz		22		pA/√Hz
	Switching Time			50		ns
XTLK	Crosstalk	Channel to channel, f = 100 MHz		−43		dBc
ISOL	Off Isolation	f = 100 MHz		−60		dBc
Static, DC Performance						
A_{VOL}	Voltage Gain	LMH6584	0.987	1.00	1.013	V/V
		LMH6585	1.98	2.00	2.02	
V_{OS}	Input Offset Voltage			±3	±18	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	See[6]		13		µV/°C
I_B	Input Bias Current	Non-Inverting[7]		−5		µA
TCI_B	Input Bias Current Average Drift	Non-Inverting[6]		4		nA/°C

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested.
(2) Room Temperature limits are 100% production tested at 25°C. Device self heating results in $T_J \geq T_A$, however, test time is insufficient for $T_J$to reach steady state conditions. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The channel bandwidth varies over the different channel combinations and with expansion. See the application section for more details.
(5) Slew Rate is the average of the rising and falling edges.
(6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(7) Negative input current implies current flowing out of the device.

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±3.3V Electrical Characteristics[1] (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, V_S = ±3.3V, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{OUT}	Output Voltage Range	R_L = 100Ω, LMH6584	−1.36, +1.38	±1.6		V
		R_L = ∞, LMH6584[8]	−1.36, +1.38	±1.6		
		R_L = 100Ω, LMH6585	−1.82, +1.9	±2.1		
		R_L = ∞, LMH6585	±2.05	±2.2		
PSRR	Power Supply Rejection Ratio			45		dB
I_{CC}	Positive Supply Current	R_L = ∞		189	250	mA
I_{EE}	Negative Supply Current	R_L = ∞		181	240	mA
	Tri State Supply Current	RST Pin > 2.0V		30	50	mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		100		kΩ
C_{IN}	Input Capacitance	Input connected to one output		9		pF
C_{IN}	Input Capacitance	Input connected to 16 outputs (Broadcast)		12		pF
R_O	Output Resistance Enabled	Closed Loop, Enabled		300		mΩ
	Output Resistance Disabled	Disabled, LMH6584		50		kΩ
	Output Resistance Disabled	Disabled, LMH6585		1.3		
CMVR	Input Common Mode Voltage Range			±0.8		V
I_O	Output Current	Sourcing, V_O = 0 V		±45		mA
Digital Control						
V_{IH}	Input Voltage High		2.0			V
V_{IL}	Input Voltage Low				0.8	V
V_{OH}	Output Voltage High			>2.2		V
V_{OL}	Output Voltage Low			<0.4		V
T_S	Setup Time			9		ns
T_H	Hold Time			9		ns

(8) This parameter is specified by design and/or characterization and is not tested in production.

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±5V Electrical Characteristics[1]

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±5V, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[3]	Max[2]	Units
Frequency Domain Performance						
SSBW	−3 dB Bandwidth	LMH6584, V_{OUT} = 0.25 V_{PP}[4]		400		MHz
		LMH6585, V_{OUT} = 0.5 V_{PP}[4]		400		
LSBW		LMH6584, V_{OUT} = 1V_{PP}, R_L = 1 kΩ[4]		400		
		LMH6585, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ[4]		400		
		LMH6584, V_{OUT} = 1V_{PP}, R_L = 150Ω[4]		400		
		LMH6585, V_{OUT} = 2 V_{PP}, R_L = 150Ω[4]		400		
GF	0.1 dB Gain Flatness	V_{OUT} = 2 V_{PP}, R_L = 150Ω		50		MHz
DG	Differential Gain	R_L = 150Ω, 3.58 MHz/ 4.43 MHz		.04		%
DP	Differential Phase	R_L = 150Ω, 3.58 MHz/ 4.43 MHz		.03		deg
Time Domain Response						
t_r	Rise Time	LMH6584, 2V Step, 10% to 90%		1.75		ns
		LMH6585, 2V Step, 10% to 90%		1.25		
t_f	Fall Time	LMH6584, 2V Step, 10% to 90%		1.5		ns
		LMH6585, 2V Step, 10% to 90%		1.1		
OS	Overshoot	2V Step		5		%
SR	Slew Rate	LMH6584, 2 V_{PP}, 40% to 60%[5]		1100		V/µs
		LMH6585, 2 V_{PP}, 40% to 60%[5]		1700		
t_s	Settling Time	2V Step, V_{OUT} Within 0.5%		10		ns
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2 V_{PP}, 5 MHz		−72		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 5 MHz		−68		dBc
e_n	Input Referred Voltage Noise	>1 MHz		12		nV/√Hz
i_n	Input Referred Noise Current	>1 MHz		22		pA/√Hz
	Switching Time			50		ns
XTLK	Crosstalk	Channel to Channel, f = 100 MHz		−43		dBc
		Channel to Channel, f = 10 MHz		−52		dBc
ISOL	Off Isolation	f = 100 MHz		−60		dBc
Static, DC Performance						
A_{VOL}	Voltage Gain	LMH6584	0.987	1.00	1.013	V/V
		LMH6585	1.98	2.00	2.02	
V_{OS}	Input Offset Voltage	Input Referred		±2	±18	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	See[6]		21		µV/°C
I_B	Input Bias Current	Non-Inverting[7]		−7	−12	µA
TCI_B	Input Bias Current Average Drift	Non-Inverting[6]		3.8		nA/°C

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested.
(2) Room Temperature limits are 100% production tested at 25°C. Device self heating results in $T_J \geq T_A$, however, test time is insufficient for $T_J$to reach steady state conditions. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The channel bandwidth varies over the different channel combinations and with expansion. See the application section for more details.
(5) Slew Rate is the average of the rising and falling edges.
(6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(7) Negative input current implies current flowing out of the device.

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±5V Electrical Characteristics[1] (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±5V, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{OUT}	Output Voltage Range	R_L = 100Ω, LMH5484	−2.75 +2.9	±3.1		V
		R_L = ∞, LMH6584	±2.9	±3.2		
		R_L = 100Ω, LMH6585	−3.1 +3.3	±3.6		
		R_L = ∞, LMH6585	±3.7	±3.9		
PSRR	Power Supply Rejection Ratio	DC	41	45		dB
XTLK	DC Crosstalk	DC, Channel to Channel	−60	−80		dB
ISOL	DC Off Isloation	DC	−72	−80		dB
I_{CC}	Positive Supply Current	R_L = ∞		210	265	mA
I_{EE}	Negative Supply Current	R_L = ∞		200	255	mA
	Tri State Supply Current	RST Pin > 2.0V		37	60	mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		100		kΩ
C_{IN}	Input Capacitance	Input connected to one output		9		pF
C_{IN}	Input Capacitance	Input connected to 16 outputs (Broadcast)		12		pF
R_O	Output Resistance Enabled	Closed Loop, Enabled		300		mΩ
	Output Resistance Disabled	Disabled, Resistance to Ground, LMH6584		50		kΩ
		Disabled, Resistance to Ground, LMH6585	1.1	1.3	1.4	
CMVR	Input Common Mode Voltage Range		±2.5	±3.1		V
I_O	Output Current	Sourcing, V_O = 0 V	±60	±80		mA
Digital Control						
V_{IH}	Input Voltage High		2.0			V
V_{IL}	Input Voltage Low				0.8	V
V_{OH}	Output Voltage High			>2.4		V
V_{OL}	Output Voltage Low			<0.4		V
T_S	Setup Time			8		ns
T_H	Hold Time			8		ns

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Connection Diagram

Top View

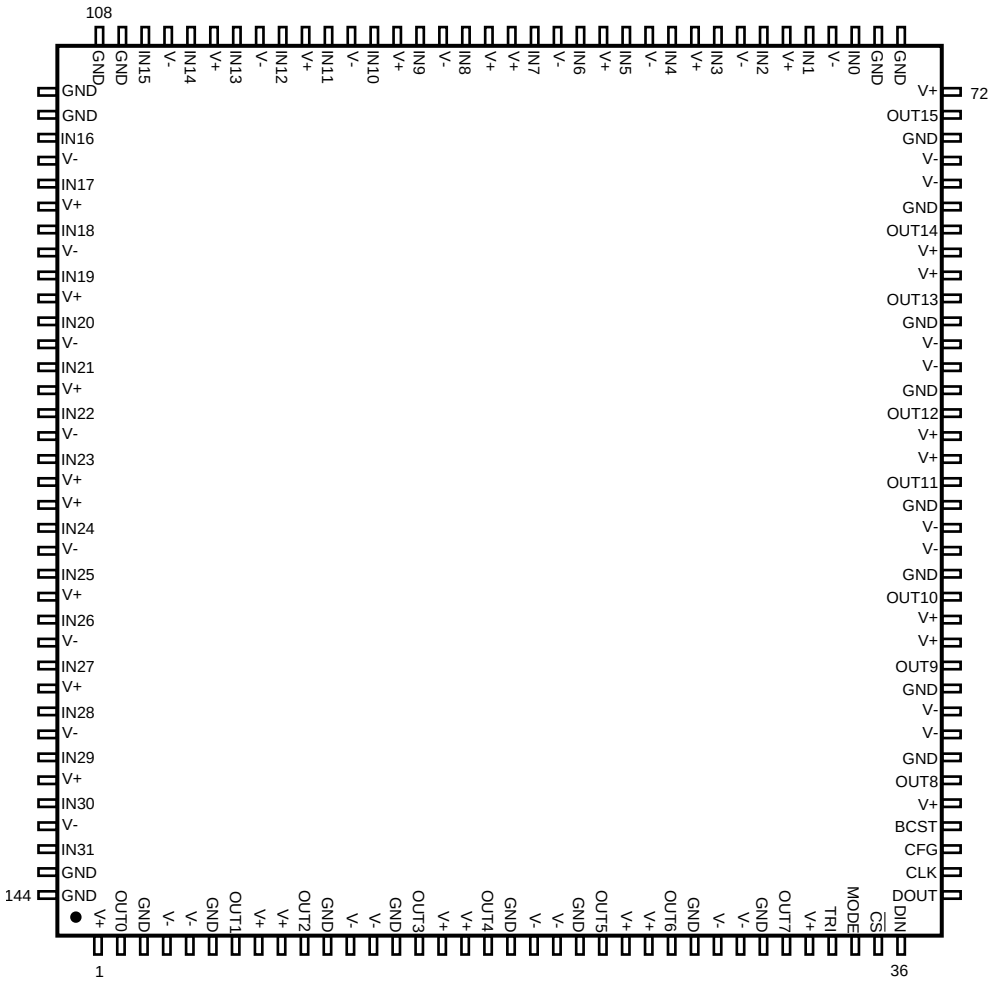


Figure 1. 144-Pin LQFP Package
See Package Number NBF0144C

Typical Performance Characteristics LMH6584

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +1, V_S = ±5V, R_L = 150Ω. **Boldface** limits apply at the temperature extremes.

1 V_{PP} Frequency Response

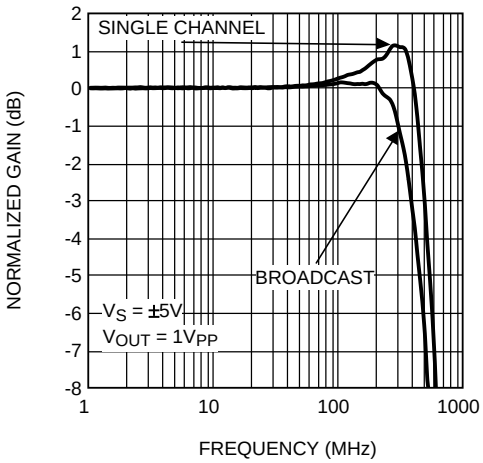


Figure 2.

1 V_{PP} Frequency Response

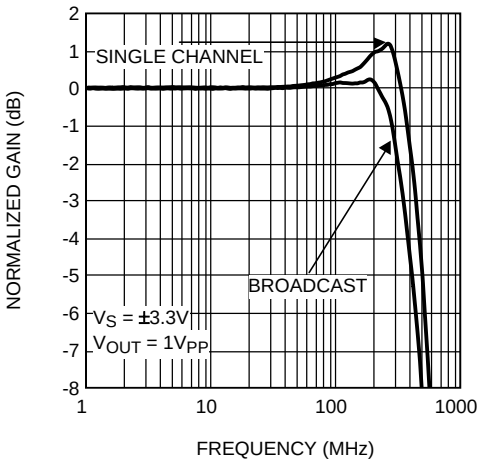


Figure 3.

Small Signal Bandwidth

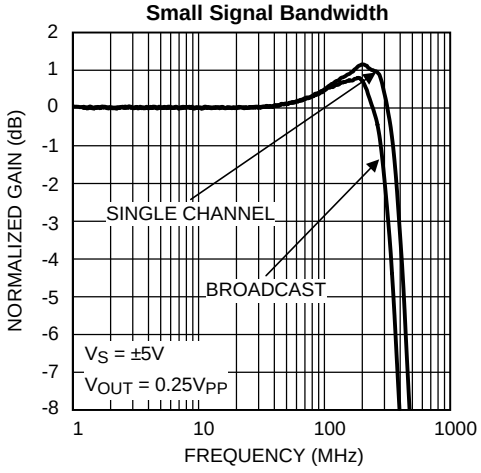


Figure 4.

Small Signal Bandwidth

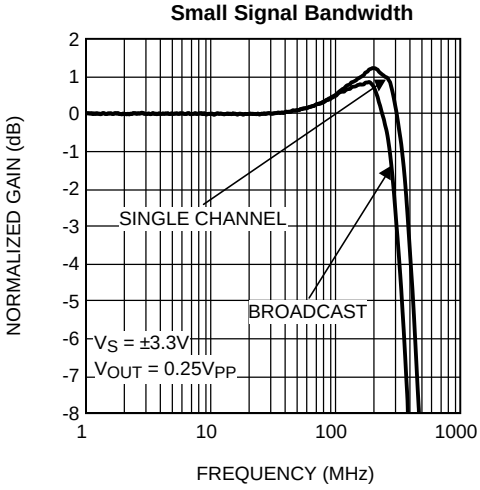


Figure 5.

Group Delay

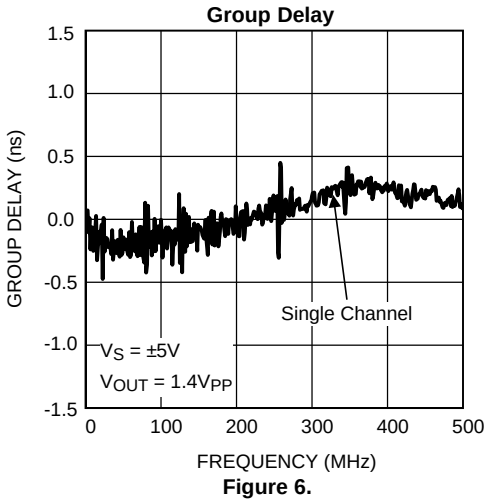


Figure 6.

Group Delay Broadcast

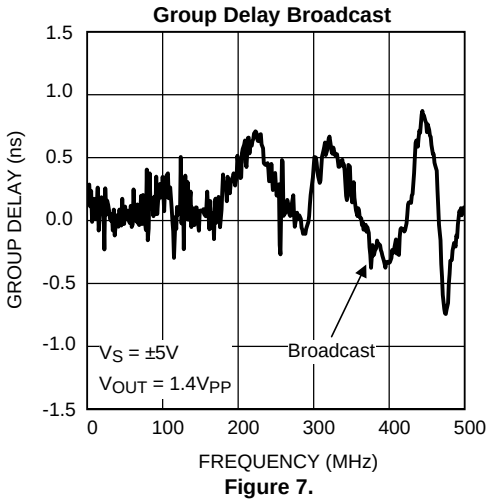


Figure 7.

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Typical Performance Characteristics LMH6584 (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +1, V_S = ±5V, R_L = 150Ω. **Boldface** limits apply at the temperature extremes.

Second Order Distortion (HD2) vs. Frequency

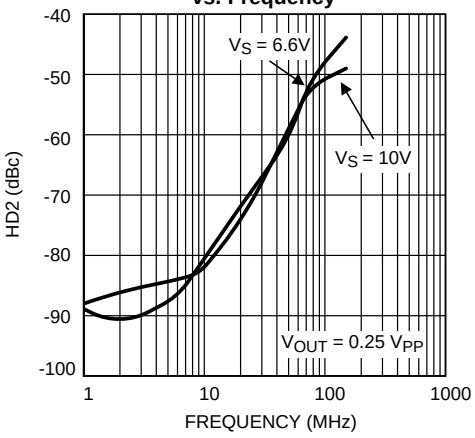


Figure 8.

Third Order Distortion (HD3) vs. Frequency

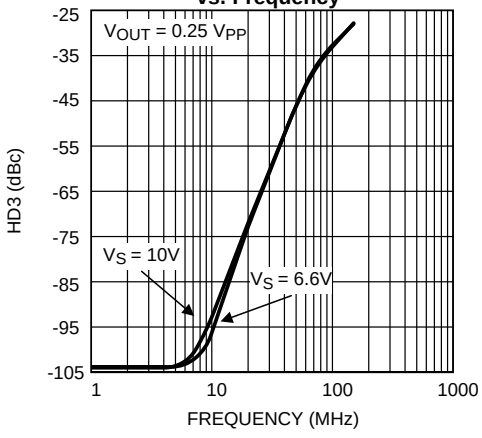


Figure 9.

Second Order Distortion vs. Frequency

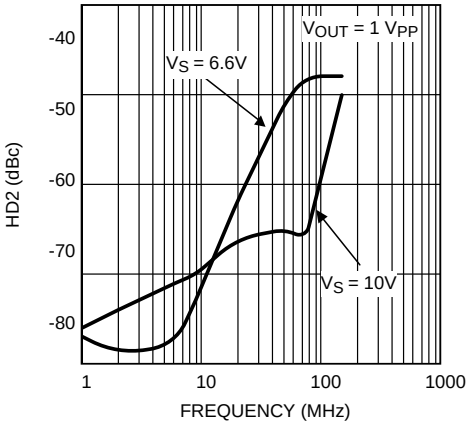


Figure 10.

Third Order Distortion vs. Frequency

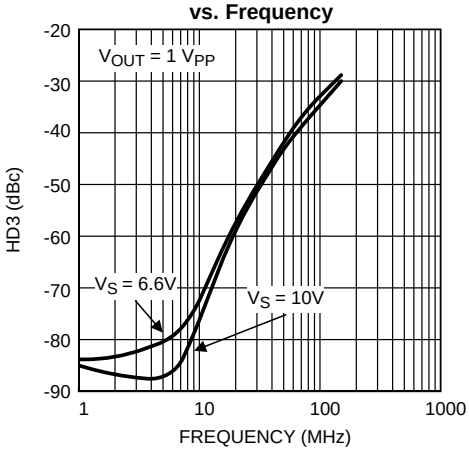


Figure 11.

Output Swing

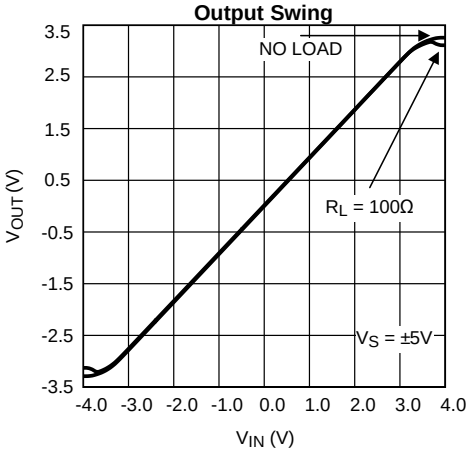


Figure 12.

Output Swing

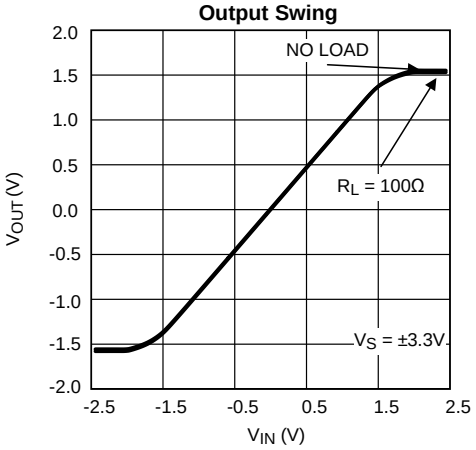


Figure 13.

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Typical Performance Characteristics LMH6584 (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +1, V_S = ±5V, R_L = 150Ω. **Boldface** limits apply at the temperature extremes.

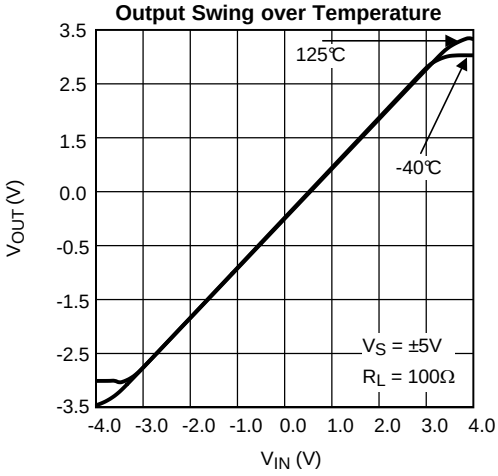


Figure 14.

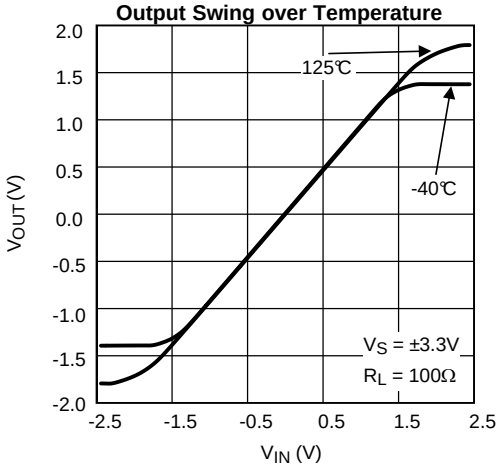


Figure 15.

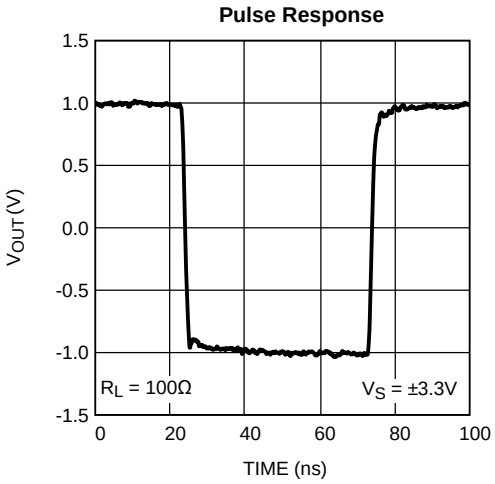


Figure 16.

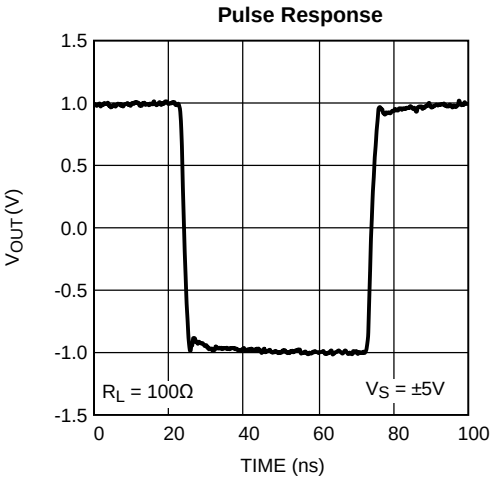


Figure 17.

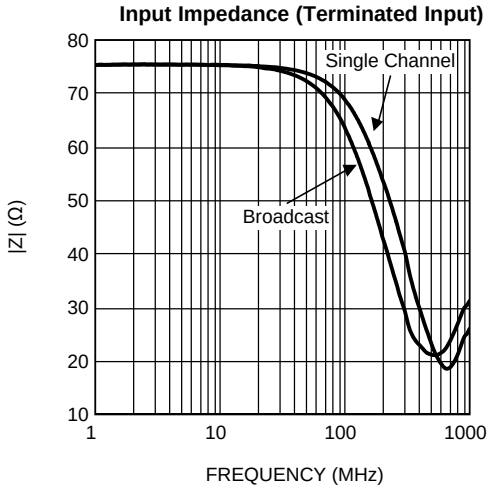


Figure 18.

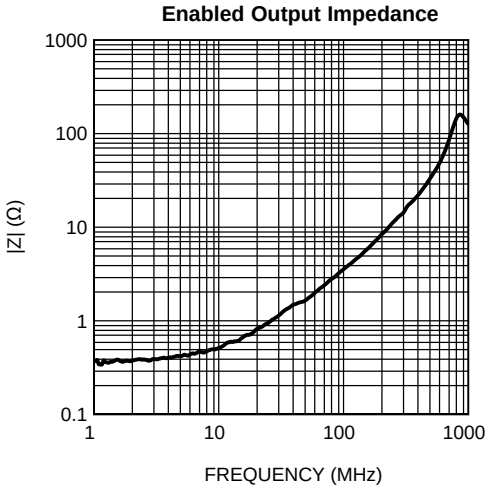


Figure 19.

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Typical Performance Characteristics LMH6584 (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +1, V_S = ±5V, R_L = 150Ω. **Boldface** limits apply at the temperature extremes.

Disabled Output Impedance

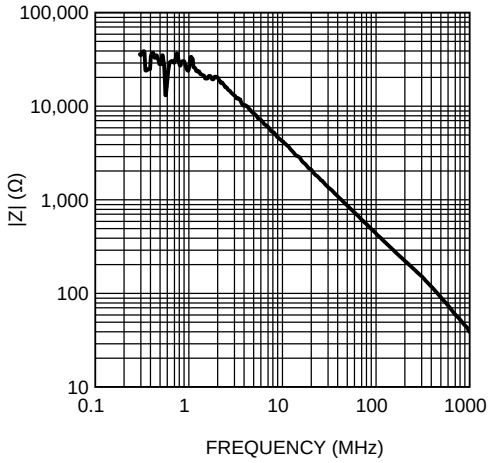


Figure 20.

Input Referred Voltage Noise

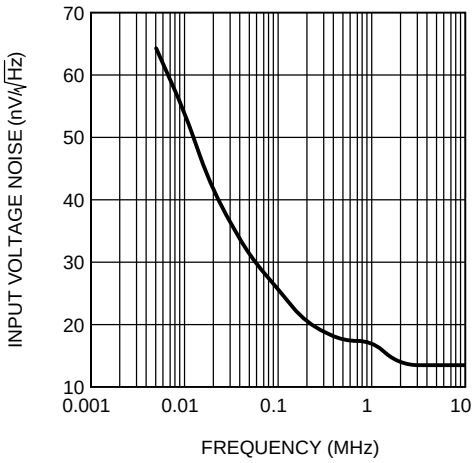


Figure 21.

Typical Performance Characteristics LMH6585

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±5V, R_L = 150Ω; **Boldface** limits apply at the temperature extremes.

2 V_{PP} Frequency Response

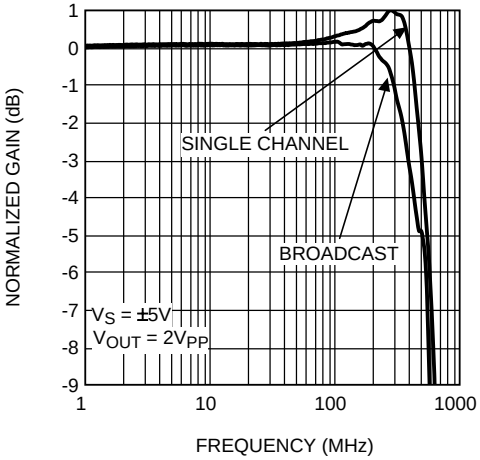


Figure 22.

2 V_{PP} Frequency Response

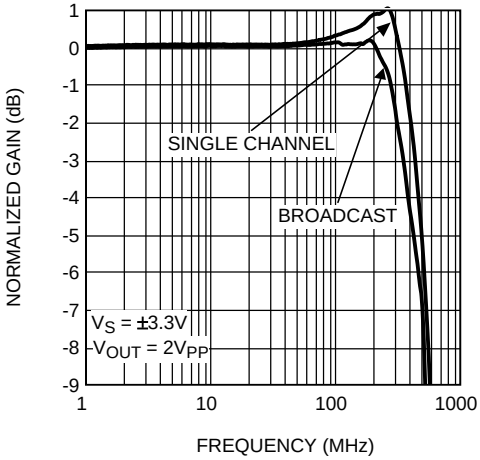


Figure 23.

Small Signal Frequency Response

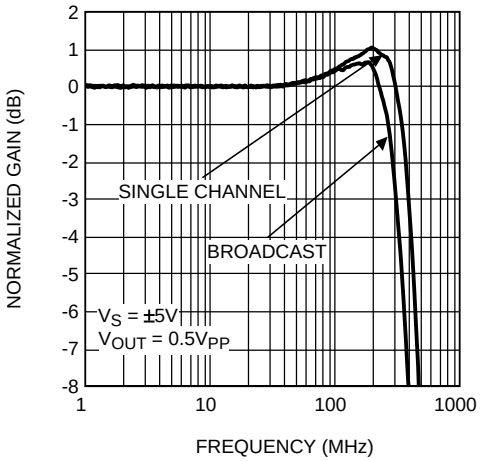


Figure 24.

Small Signal Frequency Response

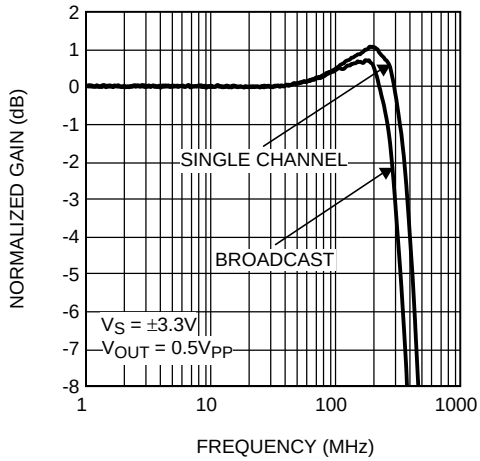


Figure 25.

Group Delay

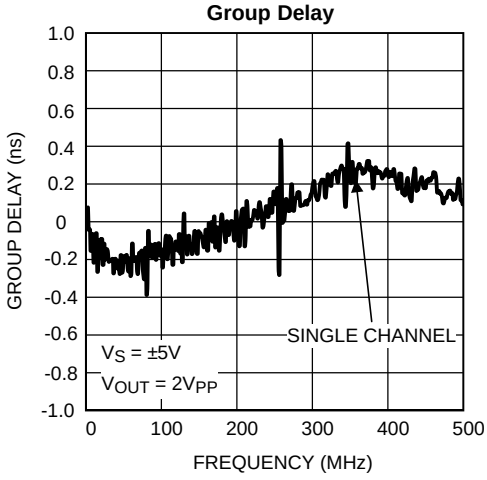


Figure 26.

Group Delay

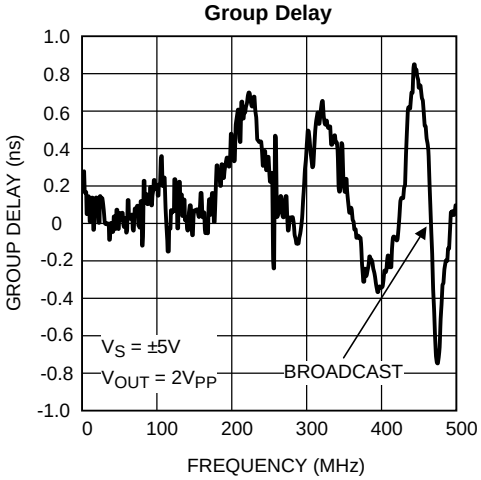


Figure 27.

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Typical Performance Characteristics LMH6585 (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±5V, R_L = 150Ω; **Boldface** limits apply at the temperature extremes.

Second Order Distortion (HD2) vs. Frequency

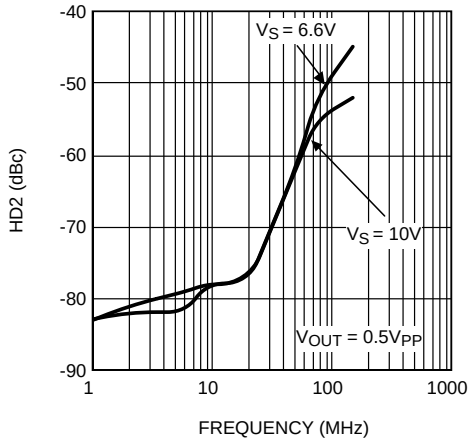


Figure 28.

Third Order Distortion (HD3) vs. Frequency

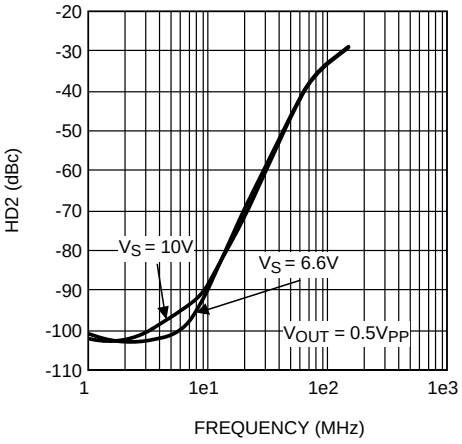


Figure 29.

Second Order Distortion (HD2) vs. Frequency

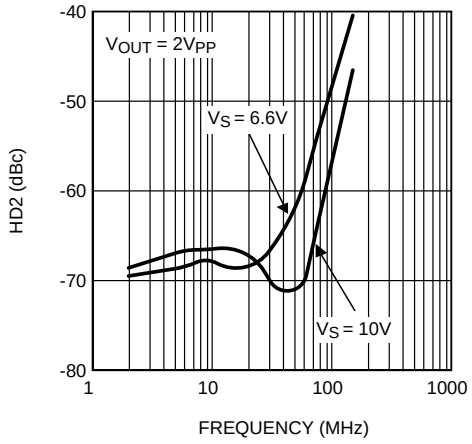


Figure 30.

Third Order Distortion (HD3) vs. Frequency

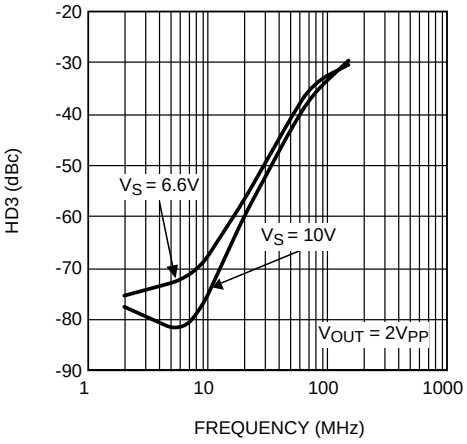


Figure 31.

Output Swing

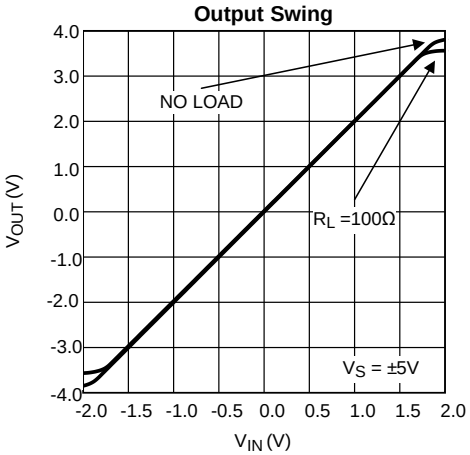


Figure 32.

Output Swing

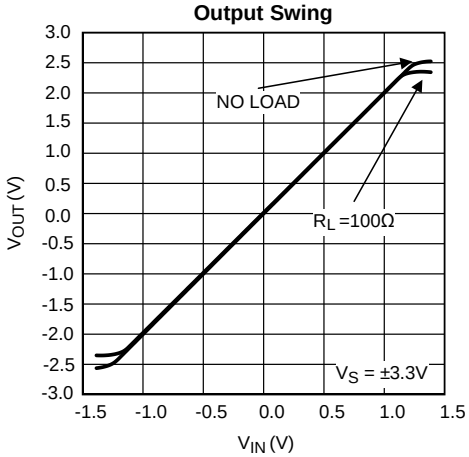


Figure 33.

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Typical Performance Characteristics LMH6585 (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±5V, R_L = 150Ω; **Boldface** limits apply at the temperature extremes.

Pulse Response

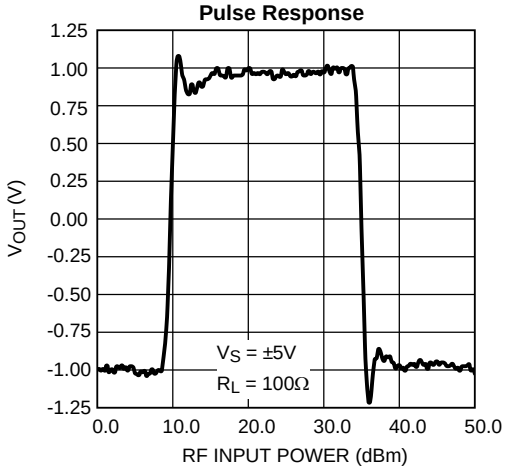


Figure 34.

Pulse Response

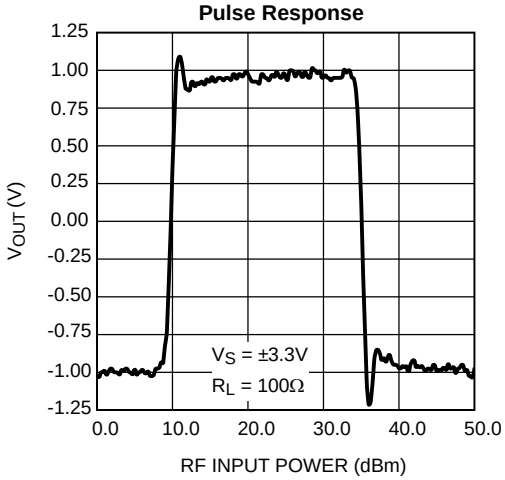


Figure 35.

Large Signal Pulse Response

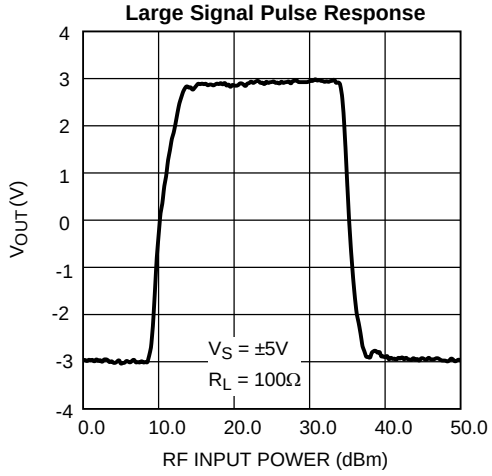


Figure 36.

Large Signal Pulse Response

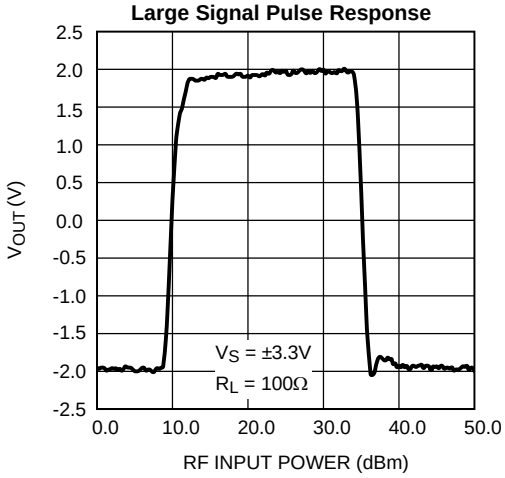


Figure 37.

Input Impedance (Terminated Input)

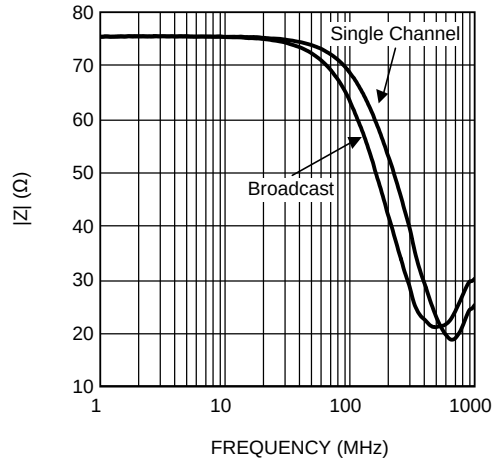


Figure 38.

Output Impedance

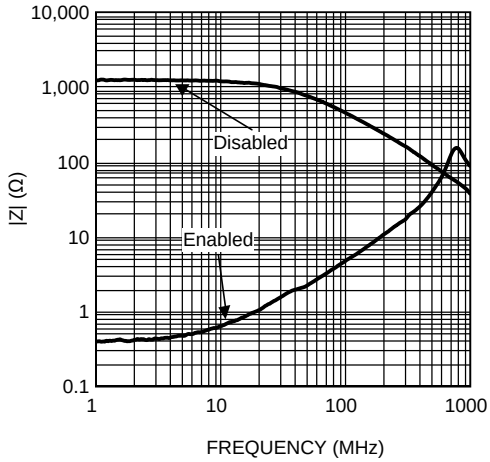


Figure 39.

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Typical Performance Characteristics LMH6585 (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±5V, R_L = 150Ω; **Boldface** limits apply at the temperature extremes.

Input Referred Voltage Noise

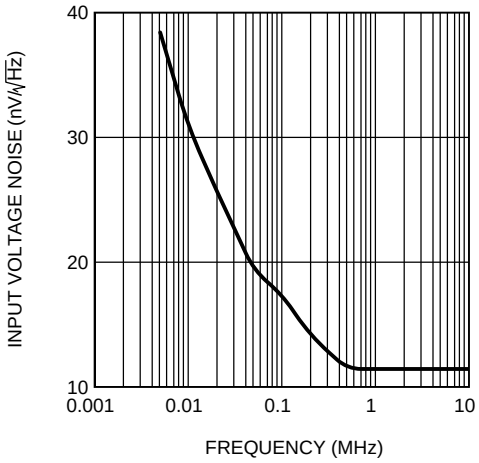


Figure 40.

APPLICATION INFORMATION

INTRODUCTION

The LMH6584/LMH6585 are high speed, fully buffered, non blocking, analog crosspoint switches. Having fully buffered inputs allow the LMH6584/LMH6585 to accept signals from low or high impedance sources without the worry of loading the signal source. The fully buffered outputs will drive 75Ω or 50Ω back terminated transmission lines with no external components other than the termination resistor. When disabled, the outputs are in a high impedance state. The LMH6584/LMH6585 can have any input connected to any (or all) output(s). Conversely, a given output can have only one associated input.

INPUT AND OUTPUT EXPANSION

The LMH6584/LMH6585 have high impedance inactive states for both inputs and outputs allowing maximum flexibility for Crosspoint expansion. In addition the LMH6584/LMH6585 employ diagonal symmetry in pin assignments. The diagonal symmetry makes it easy to use direct pin to pin vias when the parts are mounted on opposite sides of a board. As an example two LMH6584/LMH6585 chips can be combined on one board to form either an 32 x 32 crosspoint or a 64 x 16 crosspoint. To make a 32 x 32 cross-point all 32 input pins would be tied together (Input 0 on side 1 to input 31 on side 2 and so on) while the 16 output pins on each chip would be left separate. To make the 64 x 16 crosspoint, the 16 outputs would be tied together while all 64 inputs would remain independent. In the 64 x 16 configuration it is important not to have two connected outputs active at the same time. With the 32 x 32 configuration, on the other hand, having two connected inputs active is a valid state. Crosspoint expansion as detailed above has the advantage that the signal path has only one crosspoint in it at a time. Expansion methods that have cascaded stages will suffer bandwidth loss far greater than the small loading effect of parallel expansion.

Output expansion is accomplished by connecting the crosspoint inputs and leaving the output pins on both chips separate. The input capacitance of the crosspoint pins is 9pF when an input is connected to one output and 12pF when an input is connected to 16 outputs. If the crosspoint is being driven by a 75Ω transmission line the bandwidth of the circuit will be limited by the RC time constand of the transmission line and the input capacitance of the two crosspoints. In order to eliminate this bandwidth limitation it is necessary to drive the crosspoint inputs with a low impedance source. A circuit to accomplish this is show in Figure 41. The circuit shown in Figure 43 will suffer severe bandwidth limitations and is not recommended.

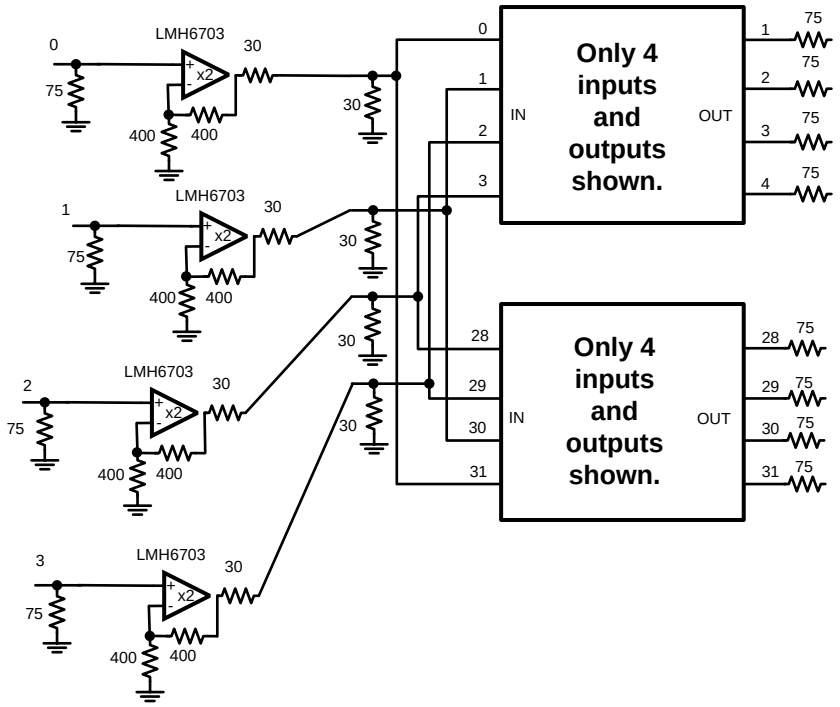


Figure 41. Output Expansion with Buffers

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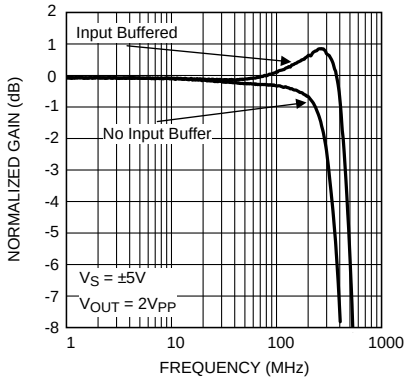


Figure 42. Frequency Response for Buffered and Unbuffered Output expansion

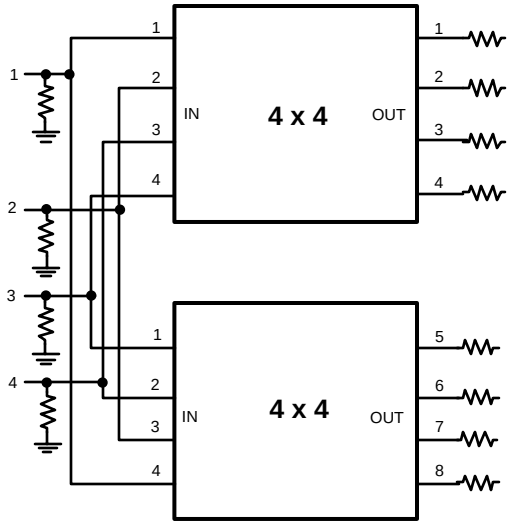


Figure 43. Output Expansion no Buffers
(Only 4 input and 4 output channels shown for illustration purposes.)

Input expansion requires more planning, is also quite easy, but there are two different options for arranging the output termination resistors. As shown in Figure 44 and Figure 45 there are two ways to connect the outputs of the crosspoint switches. In Figure 44 the crosspoint switch outputs are connected directly together and share one termination resistor. This is the easiest configuration to implement and has only one drawback. Because the disabled output of the unused crosspoint (only one output can be active at a time) has a small amount of capacitance, the frequency response of the active crosspoint will show peaking.

As illustrated in Figure 45 each crosspoint output can be given its own termination resistor. This results in a frequency response nearly identical to the non expansion case. There is one drawback for the gain of 2 crosspoint, and that is gain error. With a 75Ω termination resistor the 1250Ω resistance of the disabled crosspoint output will cause a gain error. In order to counteract this the termination resistors of both crosspoints should be adjusted to approximately 71Ω. This will provide very good matching, but the gain accuracy of the system will now be dependent on the process variations of the crosspoint resistors which have a variability of approximately ±20%.

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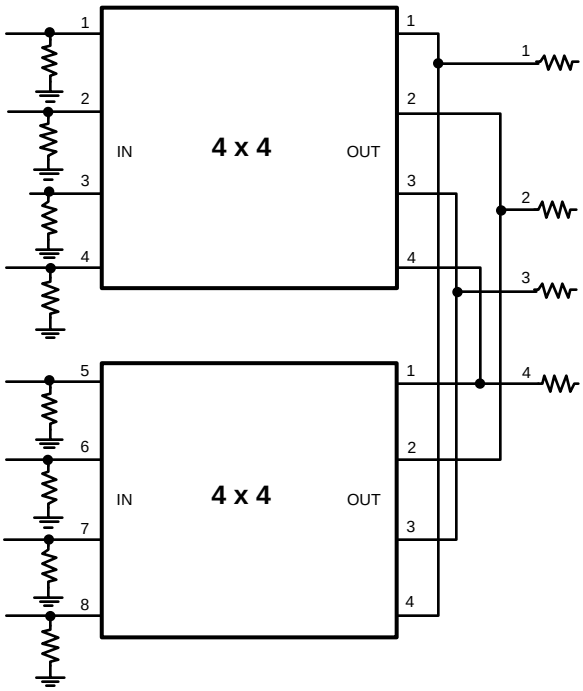


Figure 44. Input Expansion with Shared Termination Resistors (Only 4 input and 4 output channels shown for illustration purposes.)

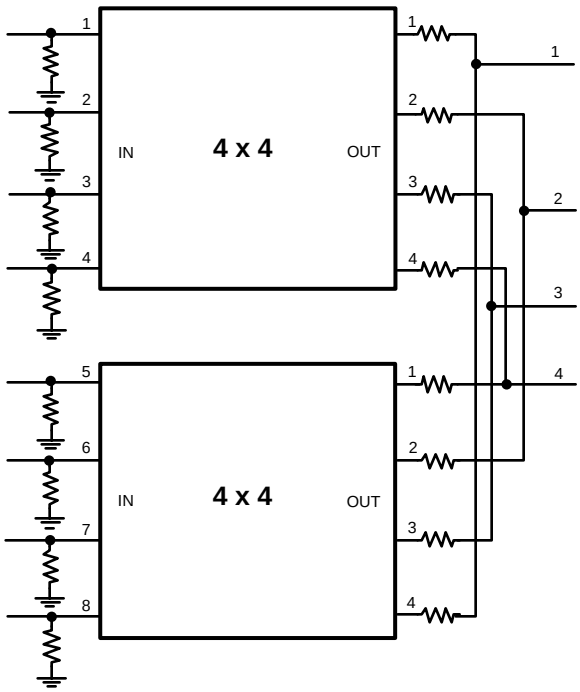


Figure 45. Input Expansion with Separate Termination Resistors (Only 4 input and 4 output channels shown for illustration purposes.)

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CHANNEL VARIATIONS

The LMH6584/LMH6584 crosspoint switches have a very large number of possible channel combinations. There is some systematic variation in channel performance. Parameters such as bandwidth and distortion have a range of values depending on which channel combination is selected. The variation in bandwidth over all possible input/output combinations is shown in Figure 46. One particular pattern to note is that input channels 0 through 3 are slower than all other inputs. The use of input buffers as illustrated above can help equalize channel bandwidths.

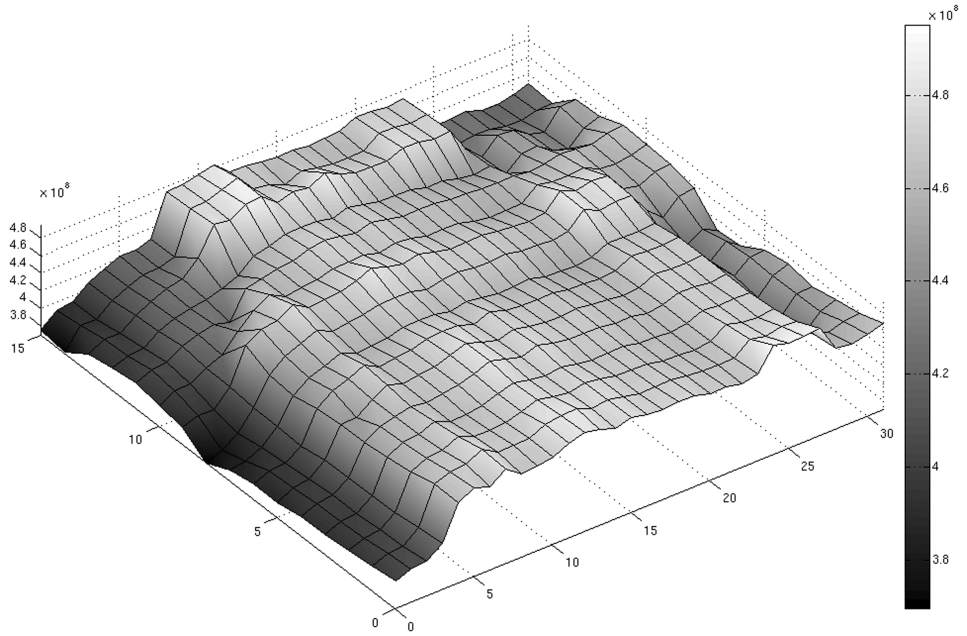


Figure 46. Bandwidth Variation over Channel Combinations

Because the inputs are the dominate factor in channel bandwidth it is possible to adjust the bandwith of the slower inputs. One method of increasing input bandwidth is with the use of buffers as illustrated in Figure 41. A simpler method using a single inductor is shown below in Figure 47.

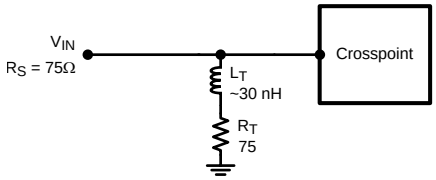


Figure 47. Use of Termination Inductor to Increase Bandwidth

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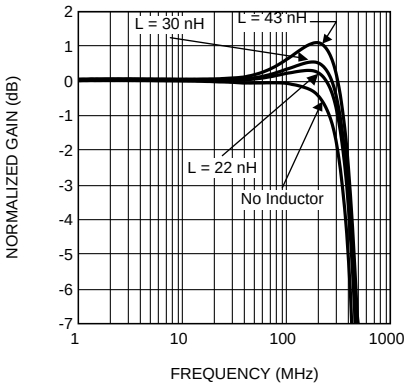


Figure 48. Termination Inductor Bandwidth Enhancement Using Input 0

The use of termination inductors can also be used when two crosspoints are used back to back for output expansion. The difference in input speeds between the opposing chips poses an additional challenge, especially if the channels that are connected together have very different performance. When connecting a slower channel (channels 0 to 3) to a faster channel the circuit shown in Figure 49 is recommended. In this case the inductor value is chosen to bring up the slow channel bandwidth, while the resistor $R_M$is used to match the performance of the two channels. Larger values of R_M will slow down the faster channel and reduce peaking. When the channels connected together are relatively well matched the matching resistor is not needed as shown in Figure 50.

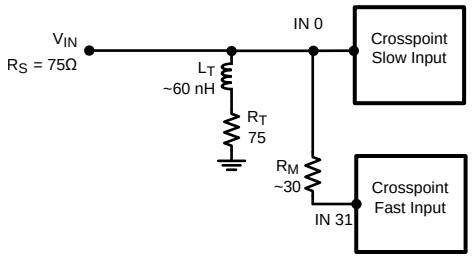


Figure 49. Inductor Termination with Mismatched Channels

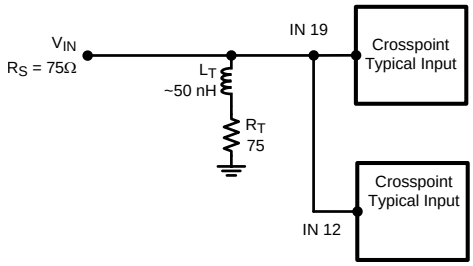


Figure 50. Inductor Termination with Matched Channels

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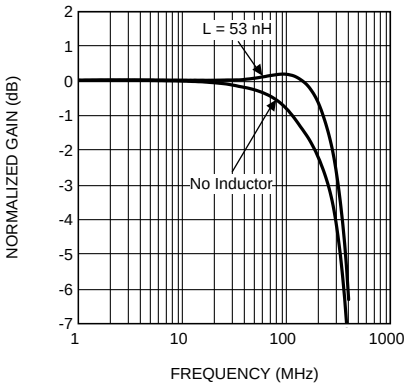


Figure 51. Termination Inductor Bandwidth Enhancement Using Input 0 Two LMH6585s Connected for Output Expansion

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. Capacitive loads of 5 pF to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. As starting values, a capacitive load of 5 pF should have around 75 Ω of isolation resistance. A value of 120 pF would require around 12Ω. When driving transmission lines the 50Ω or 75Ω matching resistor normally provides enough isolation.

USING OUTPUT BUFFERING TO ENHANCE RELIABILITY

The LMH6584/LMH6585 crosspoint switch can offer enhanced reliability with the use of external buffers on the outputs. For this technique to provide maximum benefit a very high speed amplifier such as the LMH6703 should be used, as shown in Figure 52.

The advantage offered by using external buffers is to reduce thermal loading on the crosspoint switch. This reduced die temperature will increase the life of the crosspoint. Another advantage is enhanced ESD reliability. It is very difficult to build high speed devices that can withstand all possible ESD events. With external buffers the crosspoint switch is isolated from ESD events on the external system connectors.

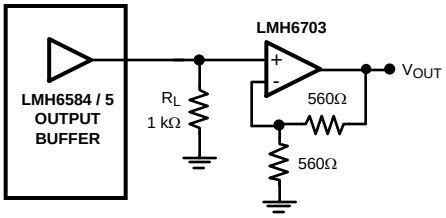


Figure 52. Buffered Output

In the example in Figure 52 the resistor R_L is required to provide a load for the crosspoint output buffer. Without R_L excessive frequency response peaking is likely and settling times of transient signals will be poor. As the value of R_L is reduced the bandwidth will also go down. The amplifier shown in the example is an LMH6703 this amplifier offers high speed and flat bandwidth. Another suitable amplifier is the LMH6702. The LMH6702 is a faster amplifier that can be used to generate high frequency peaking in order to equalize longer cable lengths. If board space is at a premium the LMH6739 or the LMH6734 are triple selectable gain buffers which require no external resistors.

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CROSSTALK

When designing a large system such as a video router, crosstalk can be a very serious problem. Extensive testing in our lab has shown that most crosstalk is related to board layout rather than the crosspoint switch. There are many ways to reduce board related crosstalk. Using controlled impedance lines is an important step. Using well decoupled power and ground planes will help as well. When crosstalk does occur within the crosspoint switch itself it is often due to signals coupling into the power supply pins. Using appropriate supply bypassing will help to reduce this mode of coupling. Another suggestion is to place as much grounded copper as possible between input and output signal traces. Care must be taken, though, not to influence the signal trace impedances by placing shielding copper too closely. One other caveat to consider is that as shielding materials come closer to the signal trace the trace needs to be smaller to keep the impedance from falling too low. Using thin signal traces will result in unacceptable losses due to trace resistance. This effect becomes even more pronounced at higher frequencies due to the skin effect. The skin effect reduces the effective thickness of the trace as frequency increases. Resistive losses make crosstalk worse because as the desired signal is attenuated with higher frequencies crosstalk increases at higher frequencies.

DIGITAL CONTROL

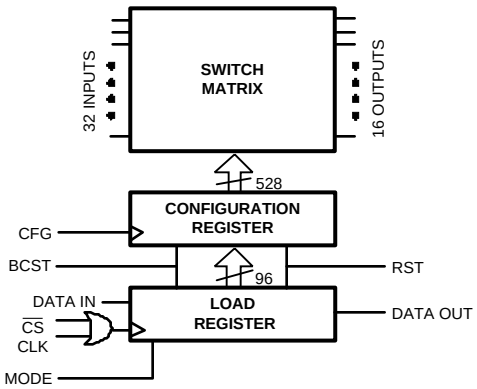


Figure 53. Block Diagram

The LMH6584/LMH6585 has internal control registers that store the programming states of the crosspoint switch. The logic is two staged to allow for maximum programming flexibility. The first stage of the control logic is tied directly to the crosspoint switching matrix. This logic consists of one register for each output that stores the on/off state and the address of which input to connect to. These registers are not directly accessible by the user. The second level of logic is another bank of registers identical to the first, but set up as shift registers. These registers are accessed by the user via the serial input bus. As described further below, there are two modes for programing the LMH6584/LMH6585, Serial Mode and Addressed Mode.

The LMH6584/LMH6585 are programmed via a serial input bus with the support of four other digital control pins. The serial bus consists of a clock pin (CLK), a serial data in pin (D_{IN}), and a serial data out pin (D_{OUT}). The serial bus is gated by a chip select pin (CS). The chip select pin is active low. While the chip select pin is high all data on the serial input pin and clock pins is ignored. When the chip select pin is brought low the internal logic is set to begin receiving data by the first positive transition (0 to 1) of the clock signal. The chip select pin must be brought low at least 5 ns before the first rising edge of the clock signal. The first data bit is clocked in on the next negative transition (1 to 0) of the clock signal. All input data is read from the bus on the negative edge of the clock signal. Once the last valid data has been clocked in, the chip select pin must go high then the clock signal must make at least one more low to high transition. Otherwise invalid data will be clocked into the chip. The data clocked into the chip is not transferred to the crosspoint matrix until the CFG pin is pulsed high. This is the case regardless of the state of the MODE pin. The CFG pin is not dependent on the state of the chip select pin. If no new data is clocked into the chip subsequent pulses on the CFG pin will have no affect on device operation.

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The programming format of the incoming serial data is selected by the MODE pin. When the MODE pin is HIGH the crosspoint can be programmed one output at a time by entering a string of data that contains the address of the output that is going to be changed (Addressed Mode). When the MODE pin is LOW the crosspoint is in Serial Mode. In this mode the crosspoint accepts a 40 bit array of data that programs all of the outputs. In both modes the data fed into the chip does not change the chip operation until the configure pin is pulsed high. The configure and mode pins are independent of the chip select pin.

THREE WIRE VS. FOUR WIRE CONTROL

There are two ways to connect the serial data pins. The first way is to control all four pins separately, and the second option is to connect the CFG and the CS pins together for a three wire interface. The benefit of the four wire interface is that the chip can be configured independently of the CS pin. This would be an advantage in a system with multiple crosspoint chips where all of them could be programmed ahead of time and then configured simultaneously. The four wire solution is also helpful in a system that has a free running clock on the CLK pin. In this case, the CS pin needs to be brought high after the last valid data bit to prevent invalid data from being clocked into the chip.

The three wire option provides the advantage of one less pin to control at the expense of having less flexibility with the configure pin. One way around this loss of flexibility would be if the clock signal is generated by an FPGA or microcontroller where the clock signal can be stopped after the data is clocked in. In this case the Chip Select function is provided by the presence or absence of the clock signal.

SERIAL PROGRAMMING MODE

Serial programming mode is the mode selected by bringing the MODE pin low. In this mode a stream of 96-bits programs all 16 outputs of the crosspoint. The data is fed to the chip as shown in the Serial Mode Data Frame tables below (four tables are shown to illustrate the pattern). The tables are arranged such that the first bit clocked into the crosspoint register is labeled bit number 0. The register labeled Load Register in the block diagram is a shift register. If the chip select pin is left low after the valid data is shifted into the chip and if the clock signal keeps running then additional data will be shifted into the register, and the desired data will be shifted out.

Also illustrated are the timing relationships for the digital pins in the Timing Diagram for Serial Mode shown below. It is important to note that all the pin timing relationships are important, not just the data and clock pins. One example is that the Chip Select pin (CS) must transition low before the first rising edge of the clock signal. This allows the internal timing circuits to synchronize to allow data to be accepted on the next falling edge. After the final data bit has been clocked in, the chip select pin must go high, then the clock signal must make at least one more low to high transition. As shown in the timing diagram, the chip select pin state should always occur while the clock signal is low. The configure (CFG) pin timing is not so critical, but it does need to be kept low until all data has been shifted into the crosspoint registers.

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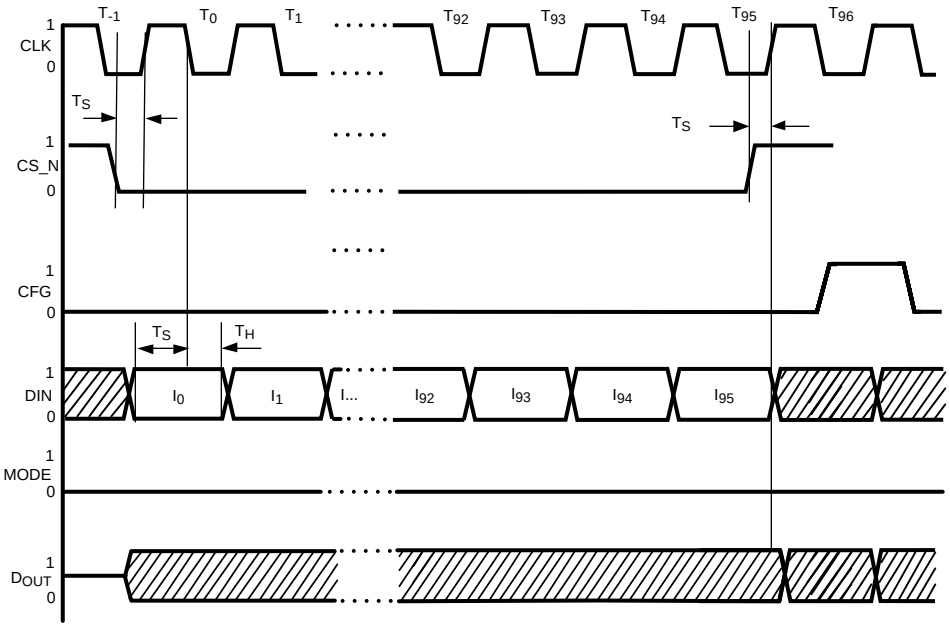


Figure 54. Timing Diagram for Serial Mode

Serial Mode Data Frame (First Two Words)(1)

Output 0						Output 1					
Input Address					On = 0	Input Address					On = 0
LSB				MSB	Off = 1	LSB				MSB	Off = 1
0	1	2	3	4	5	6	7	8	9	10	11

(1) Off = TRI-STATE, Bit 0 is first bit clocked into device.

Serial Mode Data Frame (Continued)

Output 2						Output 3					
Input Address					On = 0	Input Address					On = 0
LSB				MSB	Off = 1	LSB				MSB	Off = 1
12	13	14	15	16	17	18	19	20	21	22	23

Serial Mode Data Frame (Continued)

Output 12						Output 13					
Input Address					On = 0	Input Address					On = 0
LSB				MSB	Off = 1	LSB				MSB	Off = 1
72	73	74	75	76	77	78	79	80	81	82	83

Serial Mode Data Frame (Last Two Words)(1)

Output 14						Output 15					
Input Address					On = 0	Input Address					On = 0
LSB				MSB	Off = 1	LSB				MSB	Off = 1
84	85	86	87	88	89	90	91	92	93	94	95

(1) Bit 39 is last bit clocked into device.

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ADDRESSED PROGRAMMING MODE

Addressed programming mode makes it possible to change only one output register at a time. To utilize this mode the mode pin must be High. All other pins function the same as in serial programming mode except that the word clocked in is 8 bits and is directed only at the output specified. In addressed mode the data format is shown in the table titled Addressed Mode Word Format.

Also illustrated are the timing relationships for the digital pins in Figure 55. It is important to note that all the pin timing relationships are important, not just the data and clock pins. One example is that the Chip Select pin (CS) must transition low before the first rising edge of the clock signal. This allows the internal timing circuits to synchronize to allow data to be accepted on the next falling edge. After the final data bit has been clocked in, the chip select pin must go high, then the clock signal must make at least one more low to high transition. As shown in the timing diagram, the Chip Select pin state should always occur while the clock signal is low. The configure (CFG) pin timing is not so critical, but it does need to be kept low until all data has been shifted into the crosspoint registers.

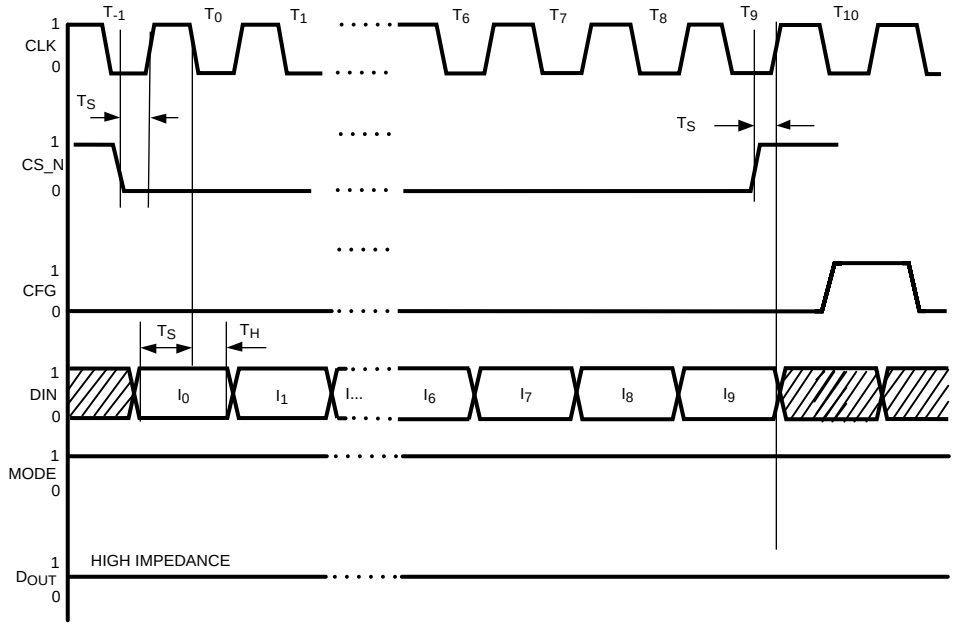


Figure 55. Timing Diagram for Addressed Mode

Table 1. Addressed Mode Word Format(1)

Output Address				Input Address					TRI-STATE
LSB			MSB	LSB				MSB	1 = TRI-STATE 0 = On
0	1	2	3	4	5	6	7	8	9

(1) Bit 0 is first bit clocked into device.

DAISY CHAIN OPTION IN SERIAL MODE

The LMH6584/LMH6585 support daisy chaining of the serial data stream between multiple chips. This feature is available only in the Serial Programming Mode. To use this feature serial data is clocked into the first chip D_{IN} pin, and the next chip D_{IN} pin is connected to the D_{OUT} pin of the first chip. Both chips may share a Chip Select signal, or the second chip can be enabled separately. When the Chip Select pin goes low on both chips a double length word is clocked into the first chip. As the first word is clocking into the first chip, the second chip is receiving the data that was originally in the shift register of the first chip (invalid data). When a full 96 bits have

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been clocked into the first chip the next clock cycle begins moving the first frame of the new configuration data into the second chip. With a full 192 clock cycles both chips have valid data and the Chip Select pin of both chips should be brought high to prevent the data from overshooting. A configure pulse will activate the new configuration on both chips simultaneously, or each chip can be configured separately. The mode, Chip Select, configure, and clock pins of both chips can be tied together and driven from the same sources.

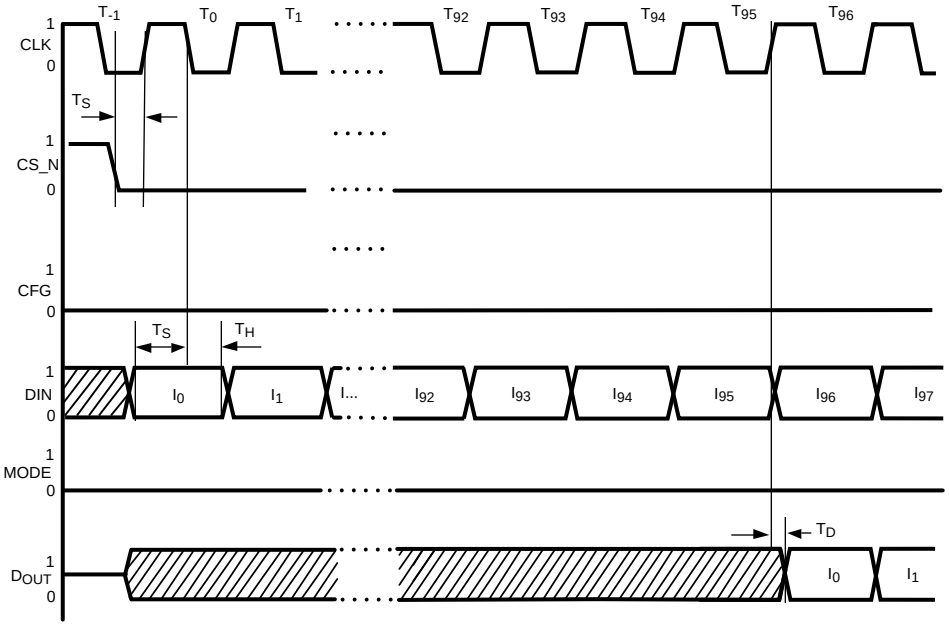


Figure 56. Timing Diagram for Daisy Chain Operation

SPECIAL CONTROL PINS

The LMH6584/LMH6585 have two special control pins that function independent of the serial control bus. One of these pins is the reset (RST) pin. The RST pin is active high meaning that at a logic 1 level the chip is configured with all outputs disabled and in a high impedance state. The RST pin programs all the registers with input address 0 and all the outputs are turned off. In this configuration the device draws only 40 mA. The reset pin can be used as a shutdown function to reduce power consumption. The other special control pin is the broadcast (BCST) pin. The BCST pin is also active high and sets all the outputs to the on state connected to input 0. Both of these pins are level sensitive and require no clock signal. The two special control pins overwrite the contents of the configuration register.

THERMAL MANAGEMENT

The LMH6584/LMH6585 are high performance device that produces a significant amount of heat. With a ±5V supply, the LMH6584/LMH6585 will dissipate approximately 2W of idling power with all outputs enabled. Idling power is calculated based on the typical supply current of 200 mA and a 10V supply voltage. This power dissipation will vary within the range of 1.8W to 2.2W due to process variations. In addition, each equivalent video load (150Ω) connected to the outputs should be budgeted 30 mW of power. For a typical application with one video load for each output this would be a total power of 2.5W. With a typical θ_{JA} of 22°C/W this will result in the silicon being 55°C over the ambient temperature. A more aggressive application would be two video loads per output which would result in 3W of power dissipation. This would result in a 66°C temperature rise. The QFP package thermal performance can be significantly enhanced with an external heat sink and by providing for moving air ventilation. Also, be sure to calculate the increase in ambient temperature from all devices operating in the system case. Because of the high power output of this device, thermal management should be considered very early in the design process. Generous passive venting and vertical board orientation may avoid the need for fan cooling provided a large heat sink is used. Also, the LMH6584/LMH6585 can be operated with a ±3.3V power supply. This will cut power dissipation substantially while only reducing bandwidth by about 10% (2 V_{PP} output). The LMH6584/LMH6585 are fully characterized and factory tested at the ±3.3V power supply condition for applications where reduced power is desired.

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The recommended heat sink is AAVD/Thermalloy part # 375024B60024G. This heat sink is designed to be used with solder anchors #125700D00000G. This heat sink is larger then the LMH6584/LMH6585 package in order to provide maximum heat dissipation, a smaller heat sink can be selected if forced air circulation will be used. With natural convection the heat sink will reduce the θ_{JA} from 22°C/W to approximately 11°C/W. Using a fan will increase the effectiveness of the heat sink considerably by reducing θ_{JA} to approximately 5°C/W. When doing thermal design it is important to note that everything from board layout to case material and case venting will impact the actual θ_{JA} of the total system. The θ_{JA} specified in the datasheet is for a typical board layout with external case enclosing the board.

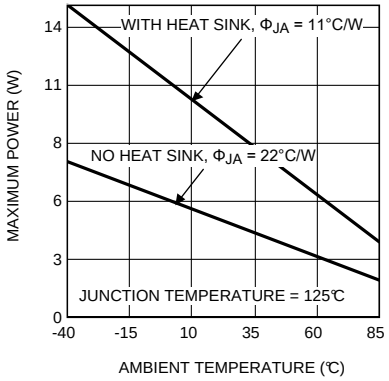


Figure 57. Maximum Dissipation vs. Ambient Temperature

PRINTED CIRCUIT LAYOUT

The LMH6584/ LMH6585 crosspoint switches are offered in a layout friendly LQFP package. With leads around the device periphery it is easier to place termination resistors and decoupling capacitors close to the device leads. Keeping power and signal traces short is crucial to high frequency performance.

Generally, a good high frequency layout will keep power supply and ground traces away from the input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 (SNOA367) for more information). If digital control lines must cross analog signal lines (particularly inputs) it is best if they cross perpendicularly. Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization Texas Instruments offers an evaluation board which can be found on the LMH6584 and LMH6585 Product Folder.

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REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	27

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6585VV/NOPB	ACTIVE	LQFP	NBF	144		TBD	Call TI	Call TI	-40 to 85	LMH6585VV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

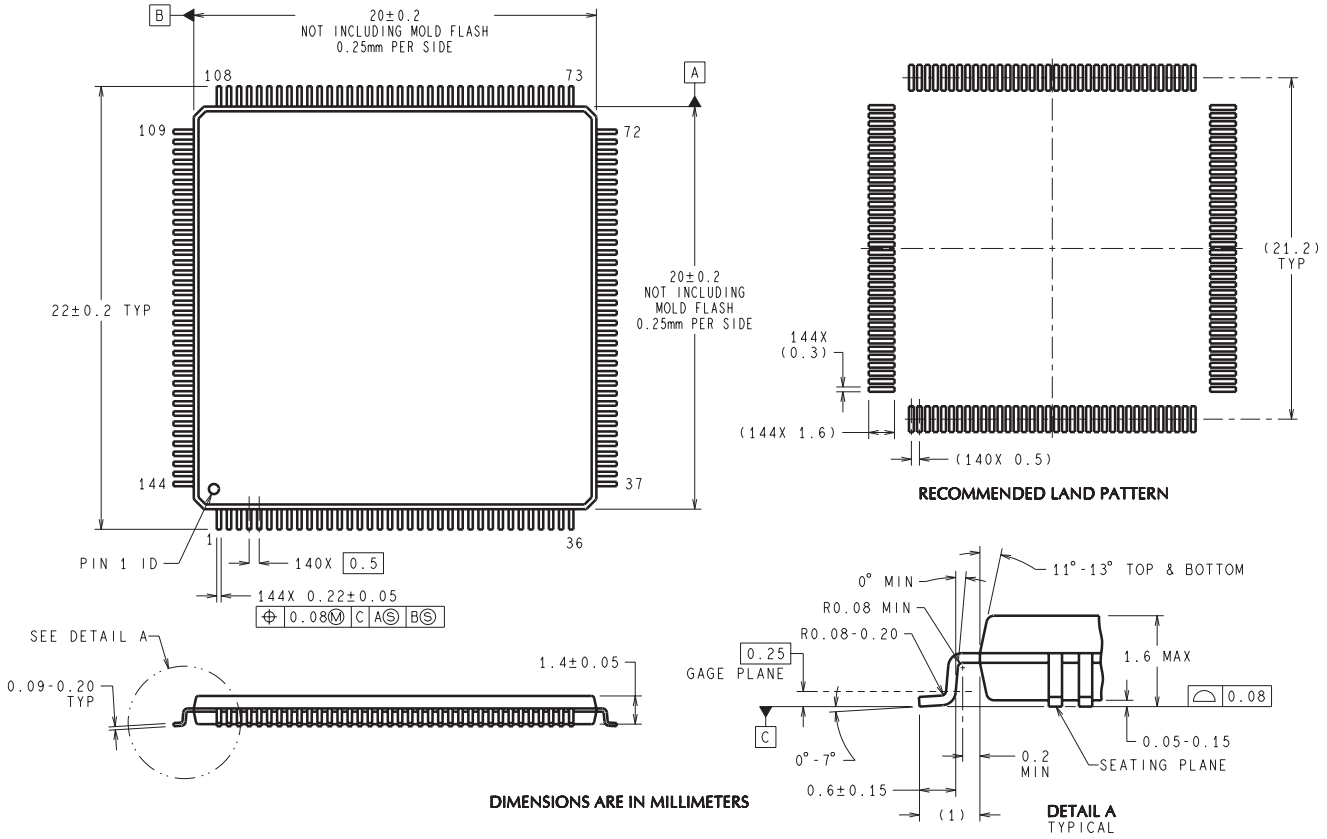
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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